**WHAT IS CLAIMED IS:**

1. An array substrate, comprising:

a substrate;

a first gate shorting bar on the substrate, the first gate shorting bar having a plurality of first connecting contact holes;

a second gate shorting bar spaced apart from and parallel to the first gate shorting bar, the second gate shorting bar having a plurality second connecting contact holes;

a plurality of gate lines on the substrate and perpendicular to the first and second gate shorting bars, the gate lines comprising odd numbered gate lines and even numbered gate lines;

a plurality of gate pads comprising odd numbered gate pads connected to the ends of odd numbered gate lines and even numbered gate pads connected to the ends of even numbered gate lines, wherein each gate pad of said plurality of gate pads has a corresponding gate pad contact hole;

a plurality of first pad connectors, each connecting an odd numbered gate pad to the first gate shorting bar via the corresponding gate pad contact hole and via a corresponding first connecting contact hole; and

a plurality of second pad connectors, each connecting an even numbered gate pad to the second gate shorting bar through the corresponding gate pad contact hole and via a corresponding second connecting contact hole.

2. The array substrate according to claim 1, wherein the plurality of gate lines include copper (Cu).

3. The array substrate according to claim 1, further including:

a plurality of data lines that cross the plurality of gate lines so as to define a plurality of pixel regions;

a plurality of thin film transistors, each thin film transistor having an associated pixel region; and

a plurality of pixel electrodes, wherein each pixel electrode is located within an associated pixel region.

4. The array substrate according to claim 3, wherein each thin film transistor includes a gate electrode, a source electrode and a drain electrode.

5. The array substrate according to claim 3, wherein the first pad connectors, the second pad connectors, and the plurality of pixel electrodes are formed of a transparent conductive material.

6. The array substrate according to claim 5, wherein the transparent conductive material includes at least one material from a group consisting of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

7. A method of fabricating an array substrate, comprising:

forming a first metal layer on a substrate;

patterning the first metal layer to form a first gate shorting bar, a vertical pattern, a plurality of odd gate lines, each having an associated odd gate pad and gate electrodes, and a plurality of even gate lines, each having an associated even gate pad and gate electrodes, wherein the vertical pattern electrically connects the odd gate pads and the even gate pads together;

forming a gate insulation layer over the substrate and over the patterned first metal layer;

forming an active layer and an ohmic contact layer over each gate electrode;

forming a second metal layer over the gate insulation layer and over the ohmic contact layers;

patterning the second metal layer to form a second shorting bar and a plurality of data lines, a plurality of source electrodes, and a plurality of drain electrodes, wherein each source electrode and each drain electrode is formed over an associated ohmic contact layer;

forming a passivation layer over the patterned second metal layer;

patterning the passivation layer to form drain contact holes to the drain electrodes, odd gate pad contact holes to the odd gate pads, even gate pad contact holes to the even gate pads, first connecting contact holes to the first gate shorting bar, second connecting contact holes to the second gate shorting bar, and etching holes to the vertical pattern;

forming a transparent conductive layer over the patterned passivation layer; and

patterning the transparent conductive layer to form pixel electrodes, first pad connectors that electrically connect the first gate shorting bar to associated odd gate pads via the first connecting contact holes and via the odd gate pad contact holes, and second pad

connectors that electrically connect the second gate shorting bar to associated even gate pads via the second connecting contact holes and via the even gate pad contact holes;

wherein patterning the transparent conductive layer etches the vertical pattern via the etching holes such that the odd gate pads are electrically isolated from the even gate pads.

8. The method of fabricating an array substrate according to claim 7, wherein the odd gate pads are arranged along an end of the odd gate lines, wherein the even gate pads are arranged along an end of the even gate lines, and wherein the first gate shorting bar is spaced apart from and parallel to the vertical pattern.

9. The method of fabricating an array substrate according to claim 7, wherein each source electrode extends from an associated data line, and wherein each drain electrode is spaced apart from an associated source electrode.

10. The method of fabricating an array substrate according to claim 7, wherein forming a first metal layer on a substrate includes depositing copper (Cu).

11. The method of fabricating an array substrate according to claim 7, wherein forming a transparent conductive layer includes depositing a material selected from a group consisting of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

12. The method of fabricating an array substrate according to claim 7, wherein patterning the transparent conductive layer forms pixel electrodes that connect with associated drain electrodes via the drain contact holes.

13. The method of fabricating an array substrate according to claim 7, further including testing the array substrate for opens or shorts.

14. The method of fabricating an array substrate according to claim 13, wherein testing the array substrate for opens or shorts includes applying voltages to the odd gate lines and to the even gate lines.

15. The method of fabricating an array substrate according to claim 14, further including cutting the first pad connectors and the second pad connectors after testing.

16. The method of fabricating an array substrate according to claim 15, further including electrically connecting a tape carrier package the odd gate pads and to the even gate pads.

17. The method of fabricating an array substrate according to claim 16, wherein electrically connecting a tape carrier package to the odd gate pads and to the even gate pads includes contacting the cut first pad connectors and contacting the cut second pad connectors.

18. The method of fabricating an array substrate according to claim 16, wherein electrically connecting a tape carrier package to the odd gate pads and to the even gate pads

includes forming an anisotropic conductive film on the cut first pad connectors and on the cut second pad connectors.